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09/883,449	06/18/2001	Nai-Yin Sung	TS00-415	2688

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EXAMINER	
TRIMMINGS, JOHN P	

ART UNIT	PAPER NUMBER
2133	3

DATE MAILED: 10/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/883,449	SUNG ET AL.	
	Examiner	Art Unit	
	John P Trimmings	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/18/2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *6/18/01* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *1, 2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: FIG. 4, 96. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: FIG. 6, 132. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities: On page 3 of the specification, line 5, the words "The BIST circuit 14..." should most likely read "The BIST circuit 10..."

Appropriate correction is required.

4. The disclosure is objected to because of the following informalities: On page 18 of the specification, line 5, the words "...further machine encoded 120..." should most likely read "...further machine encoded 132..."

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1 - 4 are rejected under 35 U.S.C. 102(b) as being fully anticipated by Bo Lu, U.S. Patent No. 6012157.

As per claim 1:

Lu teaches in the Abstract and column 5 lines 1-21 a "method of verifying the effectiveness of a RAM BIST..." by "...introducing known fault data into a RAM system model..." and "...simulating the performance of the RAM memory and the RAM BIST..." In the specifications in column 3 lines 28-38 of Lu, it completely describes and teaches the embodiment of the fault data as having three parts; (1) fault severity including BIST controller state, (2) address of fault, and (3) mask values, which determine stuck at 1, 0, or data good. These specifications described by Lu are fully the same as the finite state machine being specified in the applicant's specification on page 17, paragraph 1. And finally, Lu in column 5 lines 1-21 teaches that there is "...comparing the results of said RAM system model with said known fault data." All of the above limitations

are taught by Lu, and are applied towards claim 1 of the applicant as being fully anticipated by Lu.

As per claim 2:

Lu teaches in column 3 lines 45-48 that the fault file comprises of a "...record for each of the addresses...". According to the Microsoft Computer Dictionary, 3rd edition, 1997, a "database" file is defined as "A file composed of records..." Therefore, Lu teaches that the fault file is a database file, as is claimed by the applicant.

As per claim 3:

Lu teaches in column 2 lines 59-63 of his specification, "Modeling RAM behavior...can be performed by any type of modeling tool. However, a hardware modeling language such as VHDL currently provides the most efficient means of carrying out the invention." Therefore, Lu completely teaches the use of VHDL in the memory behavior model.

As per claim 4:

Lu teaches in his column 5 lines 21-25 that the mask values (set of faults) in the fault database "...indicating bit faults..." in the form of "stuck" 1's or 0's. Therefore, Lu teaches all of the points in the applicant's claim 4.

7. Claims 13 - 17 are rejected under 35 U.S.C. 102(b) as being fully anticipated by Bo Lu, U.S. Patent No. 6012157.

As per claim 13:

Lu teaches in the Abstract and column 6 lines 45-48 an "apparatus for verifying the effectiveness of a RAM BIST..." by "...introducing known fault data

into a RAM system model..." and "...simulating the performance of the RAM memory and the RAM BIST..." In column 3 lines 28-38 of Lu, it completely describes the embodiment of the fault data as having three parts; (1) fault severity including BIST controller state, (2) address of fault, and (3) mask values, which determine stuck at 1, 0, or data good. This is fully the same as the entire function of the finite state machine being claimed in the applicant's specification on page 17, paragraph 1. And finally, Lu in column 6 lines 45-46 teaches that there is "...comparing the results of said RAM system model with said known fault data."

As per claim 14:

Lu teaches in column 3 lines 45-48 that the fault file comprises of a "...record for each of the addresses...". According to the Microsoft Computer Dictionary, 3rd edition, 1997, a "database" file is defined as "A file composed of records...". Therefore, Lu teaches that the fault file is a database file, as is also claimed by the applicant.

As per claim 15:

Lu teaches in column 2 lines 59-63 of his specification, "Modeling RAM behavior...can be performed by any type of modeling tool. However, a hardware modeling language such as VHDL currently provides the most efficient means of carrying out the invention." Therefore, Lu teaches the use of VHDL in the memory behavior model.

As per claim 16:

Lu teaches in column 6 lines 47-51 that the mask values (set of faults) in the fault database "...indicating bit faults..." in the form of "stuck" 1's or 0's. Therefore, Lu teaches all of the points in the applicant's claim 16.

As per claim 17:

Lu teaches in his specification in column 4, lines 4 to 9 the execution by the BIST controller of a diagnostic program named 14N March. This diagnostic is also commonly referred to as March C+ (see "SynTest Enters the BIST Product", SynTest Technolgies, Inc., March 1999, http://www.syntest.com/PressReleaseArchive/19990308_2.htm), which is one of the diagnostics claimed in the applicant's claim 17.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bo Lu, U.S. Patent No. 6012157, in view SyTest Technologies, Inc., March 1999.

Lu teaches in his specification in column 4, lines 4 to 9 the execution by the BIST controller of a diagnostic program named "14N March". Lu fails to describe this diagnostic as "March C+" as the applicant specifies in the application. But, this diagnostic, 14N March, is defined and referred to also as "March C+" by SynTest Technologies (see "SynTest Enters the BIST Product", SynTest Technolgies, Inc., March 1999, http://www.syntest.com/PressReleaseArchive/19990308_2.htm). Therefore, SynTest teaches the use of the diagnostic March C+ in the specification above by Lu.

11. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bo Lu, U.S. Patent No. 601215, in view of Takahashi Ohsawa, U.S. Patent No. 5748641, and further in view of Duane L. Anderson, U.S. Patent No. 4782488. Lu substantially teaches a method of verifying the effectiveness of a RAM BIST by "...introducing known fault data into a RAM system model..." and "...simulating the performance of the RAM memory and the RAM BIST..." (column 5 lines 6-15). In column 3 lines 28-38 of Lu, it completely describes the embodiment of the fault data as having three parts; (1) fault severity including BIST controller state, (2) address of fault, and (3) mask values, which determine stuck at 1, 0, or data good. This is fully the same as the entire function of the

finite state machine being claimed in the applicant's specification on page 17, paragraph 1. And finally, Lu in column 5 lines 1-21 teaches that there is "...comparing the results of said RAM system model with said known fault data." What Lu does not specifically teach is the scrambling and descrambling of address and data to and from the memory behavior model. Ohsawa (see column 2 lines 52-59) and Anderson (column 1 lines 27-47), in describing their scrambling and descrambling patents, teach that the testing of DRAM memories may include these functions in order to more completely test and verify memory. Also, in the case of simulating the entire system claimed by the applicant, it would have been a technical requirement to include descrambling of fault data because of the data/address scrambling, because only through descrambling of the scrambled information would the test results be valid. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method disclosed by Lu to include scrambling and descrambling in order to incorporate full memory testing to the extent that is described by Anderson and Oshawa. One would have been motivated by the need to couple the scramble/descramble technique as taught in the Anderson patent in order to scramble and unscramble memories such as are taught by Oshawa (see Oshawa Abstract). It would have been obvious to apply these patents to a simulator in order to fully encompass all types of memory testing scenarios.

12. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bo Lu, U.S. Patent No. 6012157, in view of Takahashi Ohsawa, U.S. Patent No.

5748641, and further in view of Duane L. Anderson, U.S. Patent No. 4782488. Lu substantially teaches a "method of verifying the effectiveness of a RAM BIST by introducing known fault data into a RAM system model and "...simulating the performance of the RAM memory and the RAM BIST..." (column 5 lines 6-15). In column 3 lines 28-38 of Lu, it completely describes the embodiment of the fault data as having three parts; (1) fault severity including BIST controller state, (2) address of fault, and (3) mask values, which determine stuck at 1, 0, or data good. This is fully the same as the entire function of the finite state machine being claimed in the applicant's specification on page 17, paragraph 1. And finally, Lu in column 5 lines 1-21 teaches that there is "...comparing the results of said RAM system model with said known fault data." What Lu does not specifically teach is the scrambling and descrambling of address and data to and from the memory behavior model. Ohsawa (column 2 lines 52-59) and Anderson, in describing their scrambling and descrambling patents, teach that the testing of DRAM memories may include these functions in order to more completely test and verify memory (see Anderson column 2 lines 27-47). Also, in the case of simulating the entire system claimed by the applicant, it would have been a technical requirement to include descrambling of fault data to reverse the effect of the data/address scrambling, because only through descrambling of the scrambled information would the test results be valid. In other words, if the entire simulation is to properly function, the fault model data must also be descrambled as is claimed by the applicant. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the

method disclosed by Lu to include scrambling and descrambling throughout the simulator in order to incorporate full memory testing to the extent that is described by Anderson and Ohsawa. One would have been motivated by the need to couple the scramble/descramble technique as taught in the Anderson patent in order to scramble and unscramble memories such as are taught by Oshawa (see Oshawa Abstract). And, it would have been obvious to apply these patents to a simulator in order to fully encompass all types of memory testing scenarios.

13. Claims 9 – 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bo Lu, U.S. Patent No. 6012157, and in view of Takahashi Ohsawa, U.S. Patent No. 5748641, and further in view of Duane L. Anderson, U.S. Patent No. 4782488.

Lu teaches in column 5 lines 1-21 and the Abstract a "method of verifying the effectiveness of a RAM BIST..." by "...introducing known fault data into a RAM system model..." and "...simulating the performance of the RAM memory and the RAM BIST..." In column 3 lines 28-38 of Lu, it completely describes the embodiment of the fault data as having three parts; (1) fault severity including BIST controller state, (2) address of fault, and (3) mask values, which determine stuck at 1, 0, or data good. This is fully the same as the entire function of the finite state machine being claimed in the applicant's specification on page 17, paragraph 1. And finally, Lu in his claim 1 teaches that there is "...comparing the results of said RAM system model with said known fault data."

As per claim 9:

Lu teaches in column 3 lines 45-48 that the fault file comprises of a "...record for each of the addresses...". According to the Microsoft Computer Dictionary, 3rd edition, 1997, a "database" file is defined as "A file composed of records...". Therefore, Lu teaches that the fault file is a database file, as is also claimed by the applicant.

As per claim 10:

Lu teaches in column 2 lines 59-63 of his specification, "Modeling RAM behavior...can be performed by any type of modeling tool. However, a hardware modeling language such as VHDL currently provides the most efficient means of carrying out the invention." Therefore, Lu teaches the use of VHDL in the memory behavior model.

As per claim 11:

Lu teaches in column 5 lines 22-25 that the mask values (set of faults) in the fault database "...indicating bit faults..." in the form of "stuck" 1's or 0's. Therefore, Lu teaches all of the points in the applicant's claim 11.

As per claim 12:

Lu teaches in his specification in column 4, lines 4 to 9 the execution by the BIST controller of a diagnostic program named 14N March. This diagnostic is also commonly referred to as March C+ (see "SynTest Enters the BIST Product", SynTest Technolgies, Inc., March 1999, http://www.syntest.com/PressReleaseArchive/19990308_2.htm), which is one of the diagnostics claimed in the applicant's claim 12.

14. Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bo Lu, U.S. Patent No. 6012157, in view of Takahashi Ohsawa, U.S. Patent No. 5748641, and further in view of Duane L. Anderson, U.S. Patent No. 4782488. Lu substantially teaches an "apparatus for verifying the effectiveness of a RAM BIST..." (column 6 lines 28-29) by "...introducing known fault data into a RAM system model..." (column 6 lines 38-39) and "...simulating the performance of the RAM memory and the RAM BIST..." (column 5 line 13). In column 3 lines 28-38 of Lu, it completely describes the embodiment of the fault data as having three parts; (1) fault severity including BIST controller state, (2) address of fault, and (3) mask values, which determine stuck at 1, 0, or data good. This is fully the same as the entire function of the finite state machine being claimed in the applicant's specification on page 17, paragraph 1. And finally, Lu in column 6 lines 27-46teaches that there is "...comparing the results of said RAM system model with said known fault data." What Lu does not specifically teach is the scrambling and descrambling of address and data to and from the memory behavior model. Ohsawa (column 2 lines 52-59) and Anderson, in describing their scrambling and descrambling patents, teach that the testing of DRAM memories may include these functions in order to more completely test and verify memory (see Anderson column 2 lines 27-47). Also, in the case of simulating the entire system claimed by the applicant, it would have been a technical requirement to include descrambling of fault data to reverse the effect of the data/address scrambling, because only through descrambling of the scrambled information would the test results be valid. In other words, if the entire

simulation is to properly function, the fault model data must also be descrambled as is claimed by the applicant. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method disclosed by Lu to include scrambling and descrambling throughout the simulator in order to incorporate full memory testing to the extent that is described by Anderson and Ohsawa. One would have been motivated by the need to couple the scramble/descramble technique as taught in the Anderson patent in order to scramble and unscramble memories such as are taught by Oshawa (see Oshawa Abstract). And, it would have been obvious to apply these patents to a simulator in order to fully encompass all types of memory testing scenarios.

15. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bo Lu, U.S. Patent No. 6012157, and in view of "SynTest Enters the BIST Product", SynTest Technolgies, Inc., March 1999, http://www.syntest.com/PressReleaseArchive/19990308_2.htm.

Lu teaches in column 5 lines 1-21 and the Abstract an "apparatus for verifying the effectiveness of a RAM BIST..." by "...introducing known fault data into a RAM system model..." (column 5 line 7) and "...simulating the performance of the RAM memory and the RAM BIST..." (column 5 line 13). In column 3 lines 28-38 of Lu, it completely describes the embodiment of the fault data as having three parts; (1) fault severity including BIST controller state, (2) address of fault, and (3) mask values, which determine stuck at 1, 0, or data good. This is fully the same as the entire function of the finite state machine

being claimed in the applicant's specification on page 17, paragraph 1. And finally, Lu in column 5 lines 19-20 teaches that there is "...comparing the results of said RAM system model with said known fault data." Lu however fails to specify the makeup of the BIST circuit model, which is specified by the applicant's claim 20 as being an RTL or gate level design. SynTest Technologies is a memory BIST Technology Company, and it conducts the business of modeling BIST's for clients. In their press release of March 1999, their BIST model was specified as being an "RTL product". Therefore, it would have been obvious to a person in the art at the time of the invention, that RTL modeling of BIST circuits is common in the marketplace. It would have been the natural choice of one versed in the art at that time to include an RTL model in the design of a BIST controller in order offer to the public an "industry standard" design. One would have been motivated by the need to offer a product to the public that was designed within a widely used design standard.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is 703-305-0714. The examiner can normally be reached on weekdays, 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 703-305-9595. The

fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-2394.

John P Trimmings
Examiner
Art Unit 2133

jpt

Gregory J. Lamarre
for
Albert DeCady
Primary Examiner